International
Journal
Of Advanced Research in Engineering & Management (IJAREM)
ISSN: 2456-2033 || PP. 10-15

Design of Low Power Programmable Pseudo Random Pattern Generator with Test Compression Capabilities using FPGA

Sheela H,
PG Student, UTL Technologies Ltd.,

Nayana M,
Lecturer, UTL Technologies Ltd.,

Dr. Siva Yellampalli,
Principal, UTL Technologies Ltd.,

Abstract: BIST is one of the DFT techniques, which has the capability to test itself. In BIST, the switching activity while scan loading contributes to the high power dissipation. This leads to increase in the overall power dissipation during the test. This paper presents a new programmable low power test compression method to reduce the switching activity during scan loading by using preselected toggling levels. This hybrid architecture results in low test power with the trade off of area. The 64 bit programmable PRPG is implemented and compared with the existing architecture. The proposed architecture resulted in approximately 25% to 30% power reduction when compared to existing architecture.

Keywords: BIST, Test Compression, Low Power Test Scan-Based Test; Toggling;

I. Introduction

The primary objective of manufacturing test is to ensure reliable and high quality semiconductor products. The semiconductor technology, design characteristics, and the design process are the key factors that will impact on testing evolution. Test engineers usually have to construct test vectors after the design is completed. This invariably requires a substantial amount of time and effort that could be avoided if testing is considered early in the design flow. As a result, integration of design and test, referred to as DFT.LBIST is one of the DFT techniques in which test circuitry will be reside along with the CUT and it has the capability to test itself. The basic LBIST architecture is shown in figure 1.

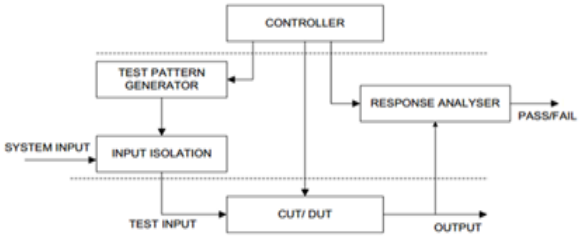

Fig.1: Architecture of BIST

The basic LBIST architecture consists of TPG(Test Pattern Generator), CUT (Circuit Under Test) , controller, ROM and analyzer. The LFSR is most commonly used TPG for LBIST. The patterns generated from the TPG are applied to the CUT. The response from the CUT is compared with the golden values which are stored in ROM. If both are same analyser gives the result as pass if not fail. The overall operation is controlled by the BIST controller.

II. Basic Architecture of PRPG

Figure 2 shows the basic structure of a PRESTO generator. An n-bit PRPG [1] connected with a phase shifter feeding scan chains [2] [3] forms a kernel of the generator producing the actual pseudorandom test patterns. A

linear feedback shift register [4] [5] [6] [2] or a ring generator can implement a PRPG [7]. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register [5]. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter [8] with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output.

As mentioned previously, the toggle control register super- vises the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, thus transparent for data arriving from the PRPG [1]. Their fraction determines a scan switching activity. The control register is reloaded once per pattern with the content of an additional shift register. The enable signals injected into the shift register are produced in a probabilistic fashion by using the original PRPG with a programmable set of weights. The weights are determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing probabilities beyond simple powers of 2. A 4-bit register Switching is employed to activate AND gates, and allows selecting a user-defined level of switching activity. For example, the switching code 0100 will set to 1, on the average, 25% of the control registers stages, and thus 25% of hold latches will be enabled. Given the phase shifter structure, one can assess then the amount of scan chains receiving constant values, and thus the expected toggling ratio.

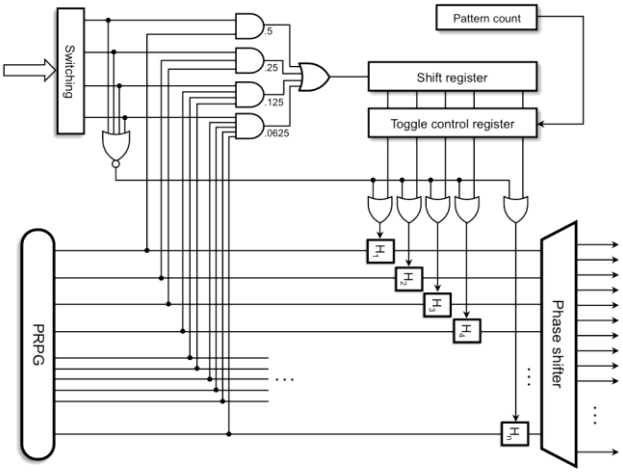

Figure 2: Basic Architecture of PRPG

An additional 4-input NOR gate detects the switching code 0000, which is used to switch the LP functionality off. It is worth noting that when working in the weighted random mode, the switching level selector ensures statistically stable content of the control register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the LP mode, though a set of actual low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable. Section III presents additional features that make the PRESTO generator [8] fully operational in a wide range of desired switching rates.

III. Existing Work

Much higher flexibility in forming low-toggling test patterns can be achieved by deploying a scheme presented in Fig. 2. Essentially, while preserving the operational principles of the basic solution, this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a T-type flip-flop [7] that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND gates on the control register

outputs to allow freezing of all phase shifter inputs. This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the control register can pass test data moving from the PRPG to the scan chains.

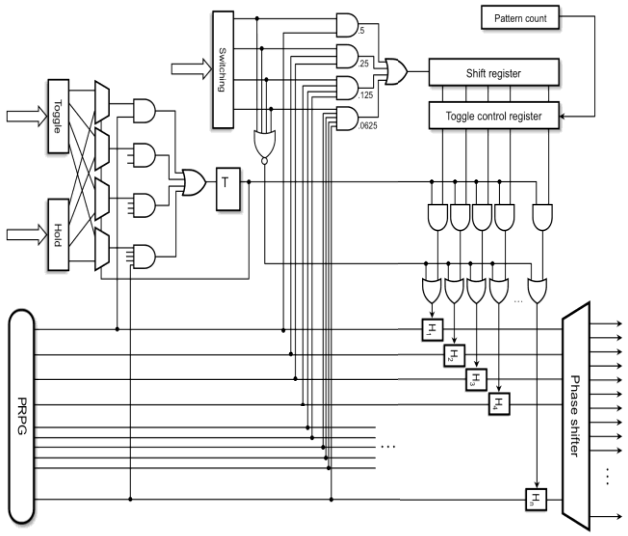

Figure 3: Block diagram of existing PRPG

Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a manner similar to that of weighted logic used to feed the shift register [9]. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator. For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register, which determines when to terminate the hold mode.

IV. PROPOSED WORK

In order to facilitate test data decompression while storing its actual functionality, the circuitry of figure 3 has to be rearchitected. This is shown in Fig 4 block diagram of LP decompressor. The main principle of the decompressor is to disable both weighted logic blocks Toggle Controller. Hold Controller and to place deterministic control data instead. In particular, the data of the toggle control register can now be chose in a deterministic manner due to a multiplexer placed below the shift register Toggle control register. Furthermore, the Toggle and Hold registers are utilized to alternately preset a 4-bit binary down counter, and thus to establish durations of the hold and toggle phases. When this circuit attains the value of zero, it originates a dedicated signal to go high in a way to toggle the T flip-flop. The same signal enables the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flip-flop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the down counter, further referred to as an offset, and determines that mode's duration.

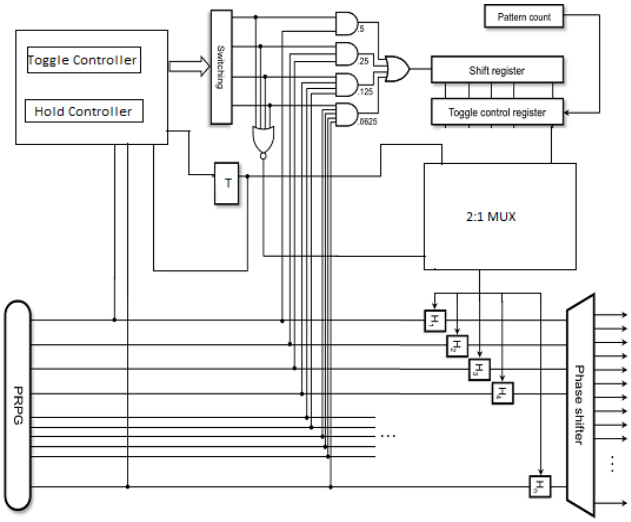

Figure 4: Block diagram of proposed low power decompressor

In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle produced at the end of the ring generator initialization phase reloads all latches with the current content of this part of the decompressor. Finally, external Automatic testing equipment (ATE) channels (feeding the original PRPG) allow one to implement a continuous flow test data decompression paradigm such as the dynamic LFSR reseeding [10]. Given the size of PRPG, the number of scan chains and the corresponding phase shifter, the switching code, the offset, as well as the values kept in the Toggle and Hold registers [7], the entire decompressor produce deterministic (decompressed) test patterns having a desired level of toggling provided the scan chains are balanced. Where as Toggle has given high priority, so that it can identify stuck at faults and circuit will be in toggle mode for desired number of period. This LP decompressor is checked with circuit under test. The Phase Shifter 64 bit output is feed into CUT. This is written in Verilog and simulated carried out in Xilinx ISIM. Xilinix ISE design suite 14.2 is used for synthesis, which gives RTL view, design summary of circuit, and total power consumption by circuit.

V. Results

This section presents simulation results obtained for the PRESTO generator shown in Fig.5, RTL View of Basic PRPG Architecture shown in Fig.6, Waveform of existing PRPG PRESTO shown in Fig.7. Designs are verified with Benchmark circuit. Involves signals prpg_out[31:0] prpg input is 64-bit LFSR, RTL Top view module shown in Fig. 8. Waveform of proposed LP Decompressor showing Hold mode. Switch[3:0] 4-bit switching register, shifter_register [64:1] shifts 64-bit data in parallel in parallel out, toggle_control_reg[63:0] 64-bit controlled data is toggled with 255-bit, hold_toggle[64:1] holds the data,ps_out[64:1]a 3-bit ex- ORed data is phase shifter output, out [24:0] by 64-bit phase shifter output is sent to benchmark circuit. Power consumption of existing architecture table is shown in figure 9 and power consumption of proposed architecture table is shown in figure 10, which is executed in Xilinx and synthesis is showing in Xilinx xpower analyzer. In basic architecture power consumption is 0.059W whereas; in proposed architecture power consumed is 0.040W.

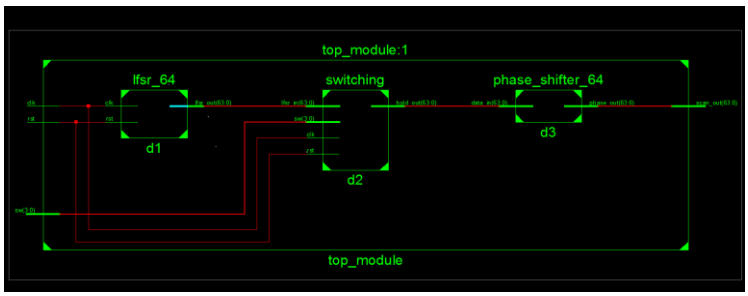

Figure 5: RTL View of Top module of Basic PRPG Architecture (PRESTO Generator)

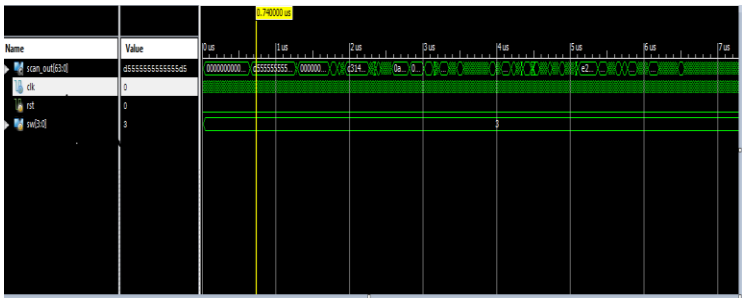

Figure 6: Simulation result of Basic PRPG Architecture

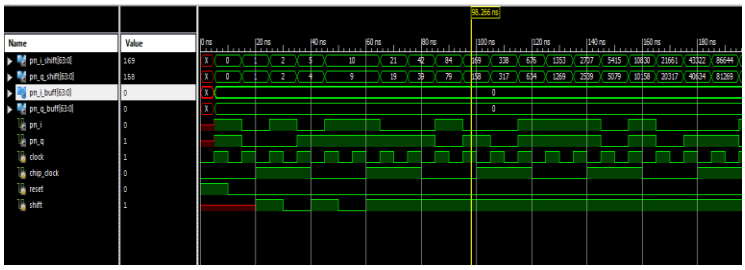

Figure 7: Simulation result of existing PRPG

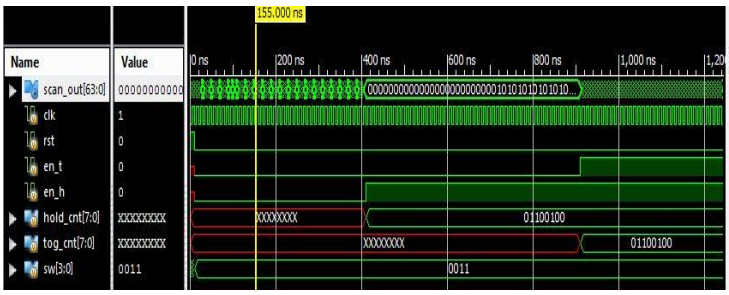

Figure 8: Simulation result of proposed decompressor

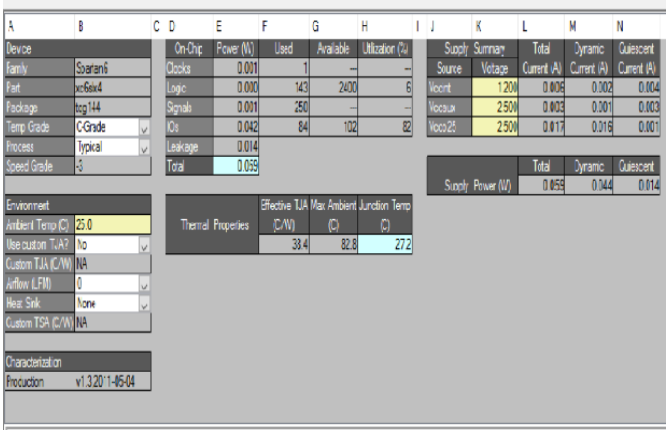

Figure 9: Table showing power consumption of existing architecture

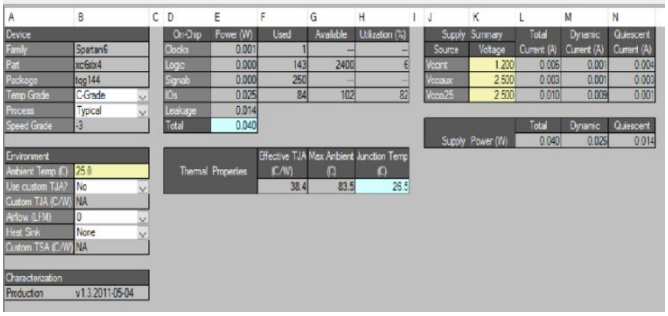

Figure 10: Table showing power consumption of proposed architecture

VI. Conclusion

The LP generator can produce pseudorandom test patterns with scan shift-in switching activity precisely selected through automated programming and having a capacity of holding and toggling a data for given period of time. This LP PRPG is also capable of acting as a fully functional test data decompressor with the ability to control scan shift-in switching activity through the process of encoding. The proposed hybrid solution allows one to efficiently combine test compression with logic BIST, where both techniques can work synergistically to deliver high quality test. In future application this can be utilized for logic BIST test pattern generator with transition controller and multiplier. The architecture presented in this architecture resulted in approximately 25% to 30% power reduction when compared to existing architecture. The patterns generated from both the architectures are same hence, fault coverage will remains same.

References

[1]. M. Filipek *et al.*, "Low power decompressor and PRPG with constant value broadcast," in *Proc. 20th Asian Test Symp. (ATS)*, Nov. 2011, pp. 84–89.

[2]. J. Rajski, J. Tyszer, G. Mrugalski, and B. Nadeau-Dostie, "Test generator with preselected toggling for low power built-in self-test," in *Proc. IEEE 30th VLSI Test Symp. (VTS)*, Apr. 2012, pp. 1–6.

[3]. R. Kapur, S. Mitra, and T. W. Williams, "Historical perspective on scan compression," *IEEE Design Test*, vol. 25, no. 2, pp. 114–120, Mar./Apr. 2008.

[4]. A. S. Abu-Issa and S. F. Quigley, "Bit-swapping LFSR for low-power BIST," *Electron. Lett.*, vol. 44, no. 6, pp. 401–402, Mar. 2008.

[5]. T. Saraswathi, K. Ragini, and C. G. Reddy, "A review on power optimization of linear feedback shift register (LFSR) for low power built in self test (BIST)," in *Proc. 3rd Int. Conf. Electron. Comput. Technol. (ICECT)*, Apr. 2011, pp. 172–176.

[6]. X. Liu and Q. Xu, "On simultaneous shift- and capture-power reduction in linear decompressor-based test compression environment," in *Proc. Int. Test Conf. (ITC)*, Nov. 2009, pp. 1–10, paper 9.3. 23,no.6, june 2015.

[7]. Michal Filipek and Nilan Mukharjee, Grzegorz Mrugalski. "Low Power Programmable PRPG with Test Compression Capabilities", IEEE transactions on Very Large Scale Integration, Vol 23,no.6, june 2015.

[8]. X. Lin and J. Rajski, "Adaptive low shift power test pattern generator for logic BIST," in *Proc. 19th IEEE Asian Test Symp. (ATS)*, Dec. 2010, pp. 355–360.

[9]. B. Singh, A. Khosia, and S. Bindra, "Power optimization of linear feedback shift register (LFSR) for low power BIST," in *Proc. IEEE Int. Adv. Comput. Conf. (IACC)*, Mar. 2009, pp. 311–314.

[10]. J. Lee and N. A. Touba, "LFSR-reseeding scheme achieving low-power dissipation during test," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no. 2, pp. 396–401, Feb. 2007.